## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

re the Application of: HASHIMOTO, Hiroshi et al.

Group Art Unit: 2714

Date: May 18, 2004

Serial No.: **09/960,399** 

**Examiner: Howard Weiss** 

Filed: September 24, 2001

P.T.O. Confirmation No.: 5652

For.

SEMICONDUCTOR INTEGRATED CIRCUIT AND FABRICATION PROCESS

**THEREOF** 

## PRELIMINARY AMENDMENT

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

Prior to calculation of the filing fee and examination of this application, please amend the above-identified patent application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments being on page 17 of this paper.